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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,348	01/08/2001	Guojin Liang	60012-0011	8149

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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2634	4

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,348	LIANG, GUOJIN	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. Claim 12 is objected to because of the following informalities: Examiner suggests applicant replace the word "date" with "data" in line 2 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10-15, 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishibashi et al. (US Patent 5, 621,774).

(1) With regard to claim 1, Ishibashi et al. discloses in Figs. 1A and 5, a receiver comprising a latching mechanism (Lin (0)-Lin (n)), coupled to receive a data stream comprising a plurality of data units (DT(0)-DT(n)), each data unit occupying a data

period, said latching mechanism latching said data units in response to latching control signals; a signal generator (11) coupled to receive a reference signal, said signal generator generating said latching control signals based upon said reference signal; and an adjustable delay element (DL(1)-DL(a)) coupled to receive a clock signal (CK) and delaying said clock signal by a variable delay to derive said reference signal, said reference signal so derived causing said signal generator to generate said latching control signals (col. 2, lines 28-37) such that each of said latching control signals coincides approximately with a midpoint of a data period (col. 2, lines 57-66; col. 8, lines 41-56).

(2) With regard to claim 2, Ishibashi et al. also discloses the receiver of claim 1, wherein said clock signal is synchronized with said data stream but is not necessarily aligned therewith (col. 4, lines 62 - col. 5, line 5; col. 10, lines 14-15).

(3) With regard to claim 3, Ishibashi et al. also discloses the receiver of claim 1, wherein said variable delay of said adjustable delay element is greater than or equal to said data period (col. 10, lines 5-9).

(4) With regard to claim 4, Ishibashi et al. also discloses the receiver of claim 1, wherein there is no more than one of said latching control signals per data period (col. 9, lines 54-63).

(5) With regard to claim 5, Ishibashi et al. also discloses in Fig. 1A, the receiver of claim 1, further comprising: a delay control mechanism (52), said delay control mechanism adjusting said variable delay imposed by said adjustable delay element to alter said reference signal, said reference signal being so altered to cause said signal generator to generate said latching control signals such that each of said latching control signals coincides more closely with a midpoint of a data period (Fig. 16; tw/2).

(6) With regard to claim 6, Ishibashi et al. also discloses wherein said delay control mechanism alters said reference signal by causing said reference signal to coincide more closely with a midpoint of a data period (col. 7, lines 54- col. 8, line 15).

(7) With regard to claim 7, Ishibashi et al. also discloses, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially a data period (col. 10, lines 5-9).

(8) With regard to claim 8, Ishibashi et al. also discloses wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period (col. 6, lines 29-61).

(10) With regard to claim 10, claim 10 inherits all limitations of claim 5, above. Furthermore Ishibashi et al. also discloses wherein said delay control mechanism comprises: a detection mechanism, said detection mechanism receiving an indication of how closely each of said latching control signals coincides with a midpoint of a data period, and providing an adjustment signal to adjust said variable delay of said adjustable delay element to alter said reference signal to cause each of said latching control signals to coincide more closely with a midpoint of a data period (col. 7, lines 54-64).

(11) With regard to claim 11, Ishibashi et al. also discloses in Figs. 5 and 6, wherein said delay control mechanism (52) further comprises: a fixed delay element coupled to receive at least one of said latching control signals and providing a delayed latching signal (CKSEL(n)); and a latching component coupled to receive said data stream, said latching component latching one of said data units in said data stream in response to said delayed latching signal (col. 6, lines 5-28).

(12) With regard to claim 12, Ishibashi et al. also discloses wherein said detection mechanism receives said one data unit from said latching component, and compares said one date unit with a plurality of data units received from said latching mechanism to determine how closely each of said latching control signals coincides with a midpoint of a data period (col. 6, line 29- col. 7, line 16; col. 8, lines 41-56).

(13) With regard to claim 13, Ishibashi et al. also discloses the receiver of claim 12, wherein said variable delay of said adjustable delay element is greater than or equal to said data period (col. 10, lines 5-9).

(14) With regard to claim 14, Ishibashi et al. also discloses the receiver of claim 13, wherein said fixed delay is approximately (X+.5) times said data period where X is an integer greater than or equal to 1 (col. 8, lines 16-56).

(15) With regard to claim 15, Ishibashi et al. also discloses wherein said detection mechanism comprises a phase detector (col. 5, lines 28-43).

(16) With regard to claim 21, Ishibashi et al. also discloses in Fig. 1A, a receiver, comprising: a latching mechanism (Lin (0)-Lin (n)), coupled to receive a data stream comprising a plurality of data units (DT(0)-DT(n)), each data unit occupying a data period, said latching mechanism latching said data units in response to latching control signals; and a signal generator coupled to receive a reference signal which is not aligned with said data stream, said signal generator (11) generating said latching control signals (col. 2, lines 28-37) based upon said reference signal such that each of said latching control signals coincides approximately with a midpoint of a data period (col. 2, lines 57-66).

(17) With regard to claim 22, claim 22 inherits all limitations of claims 21 and 3 above.

(18) With regard to claim 23, claim 23, Ishibashi et al. also discloses wherein said reference signal coincides approximately with a midpoint of a data period (col. 2, lines 57-66).

(19) With regard to claim 24, Ishibashi et al. also discloses The receiver of claim 23, wherein said reference signal is derived by delaying a clock signal, which is synchronized and aligned with said data stream, by a delay which is approximately equal to (X + .5) times said data period where X is an integer greater than or equal to 1 (col. 17-27).

(20) With regard to claim 25, claim 25 inherits all limitations of claim 23. Furthermore, Ishibashi et al. also discloses, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period (col. 6, lines 29-61).

(21) With regard to claim 26, claim 26 inherits all limitations of claim 25. Furthermore, Ishibashi et al. also discloses, wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period (col. 6, lines 29-61).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9, 16-20, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi et al. (US Patent 5,621,774) as applied to claims 1, 8 and 21 above, in view of Bedell et al. (US Patent 5,734,685).

(1) With regard to claim 9, as noted above, Ishibashi et al. discloses all limitations of claim 1 above. Ishibashi et al. does not however explicitly disclose wherein the signal generator comprises a delay locked loop.

However, Bedell discloses in Fig. 2, a clock signal deskewing system wherein the signal generator (30) comprises a delay locked loop (col. 3, lines 49-57).

One skilled in the art would have clearly recognized that a system wherein the signal generator comprises a delay locked loop is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Bedell et al. to modify the invention of Ishibashi et al. since it is well known in the art to use either phased-locked loop or delay locked loop techniques to adjust the delays on non-clock signal paths.

(2) With regard to claim 16, claim 16 inherits all limitations of claims 1 and 8 above.

(3) With regard to claim 17, Ishibashi et al. also discloses the receiver of claim 16, wherein there is no more than one of said latching control signals per data period (col. 9, lines 54-63).

(4) With regard to claim 18, Ishibashi et al. also discloses wherein said reference signal coincides approximately with a midpoint of a data period (col. 8, lines 41-56).

(5) With regard to claim 19, Ishibashi et al. also discloses wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period (col. 10, lines 5-9).

(6) With regard to claim 20, Ishibashi et al. also discloses wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period (col. 6, lines 29-61).

(7) With regard to claim 27, claim 27 inherits all limitations of claims 21 and 8 above.

7. Claims 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi et al. (US Patent 5,621,774) in view of Bedell et al. (US Patent 5,734,685).

(1) With regard to claim 28, Ishibashi et al. discloses a receiver, comprising: a latching mechanism (Lin(0)-Lin(n), coupled to receive a data stream comprising a plurality of data units (DT(0)-DT(n)), each data unit occupying a data period, said latching mechanism latching said data units in response to latching control signals; a signal generator (coupled to receive a reference signal, said delay locked loop generating said latching control signals based upon said reference signal such that each of said latching control signals coincides approximately with a midpoint of a data period (8, lines 41-56).

However, Ishibashi et al. does not disclose a delay locked loop said delay locked loop generating said latching control signals based upon said reference signal.

However, Bedell et al. teaches discloses in Fig. 2, a delay locked loop said delay locked loop generating said latching control signals based upon said reference signal (col. 3, lines 49-57).

One skilled in the art would have clearly recognized that a system wherein a delay locked loop generating said latching control signals based upon said reference signal is a well-known technique introduced in many references. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Bedell et al. to modify the invention of Ishibashi et al. since it is well known in the art to use either phased-locked loop or delay locked loop techniques to adjust the delays on non-clock signal paths.

(2) With regard to claim 29, Ishibashi et al. also discloses wherein there is no more than one of said latching control signals per data period (col. 9, lines 54-63).

(3) With regard to claim 30, Ishibashi et al. also discloses wherein said reference signal is not aligned with said data stream.

(4) With regard to claim 31, Ishibashi et al. also discloses wherein said reference signal coincides approximately with a midpoint of a data period (col. 10, lines 14-15).

(5) With regard to claim 32, Ishibashi et al. also discloses wherein said reference signal is derived by delaying a clock signal, which is synchronized and aligned with said data stream, by a delay which is approximately equal to (X + .5) times said data period where X is an integer greater than or equal to 1 (col. 8, lines 16-56).

(6) With regard to claim 33, Ishibashi et al. also discloses wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period (col. 10, lines 5-9).

(7) With regard to claim 34, Ishibashi et al. also discloses wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period (col. 6, lines 29-61).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 703-305-6969. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
May 19, 2004

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